



Product Specification

AU Optronics Corporation

() Preliminary Specification

(V) Final Specification

Module	15.4" WSXGA+ 16:10 Color TFT-LCD with LED Backlight design
Model Name	B154SW02 V3
Note ()	<i>LED Backlight without driving circuit design</i>

Customer	Date
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
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Record of Revision



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.



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2. General Description

B154SW02 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16 :10 WSXGA+, 1680(H) x 1050(V) screen and 262k colors (RGB 6-bits data driver) without LED backlight driving circuit. All input signals are LVDS interface compatible.

B154SW02 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	390.8, 15.4"			
Active Area	[mm]	331.38 x 207.11			
Pixels H x V		1680 x 3(RGB) x 1050			
Pixel Pitch	[mm]	0.19725 x 0.19725			
Pixel Format		B.G.R. Vertical Stripe			
Display Mode		Normally White			
White Luminance ($I_{LED}=20mA$) <i>(Note: ILED is LED current)</i>	[cd/m ²]	220 typ. (5 points average) 200 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		TBD			
Response Time	[ms]	16 typ / 25 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	7			
Weight	[Grams]	455 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	342.55	342.85	343.15
		Width	220.54	220.84	221.14
		Thickness	-	3.80	4.05
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-glare, Hardness 2H,			
Support Color		262K colors (RGB 6-bit)			



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Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -25 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

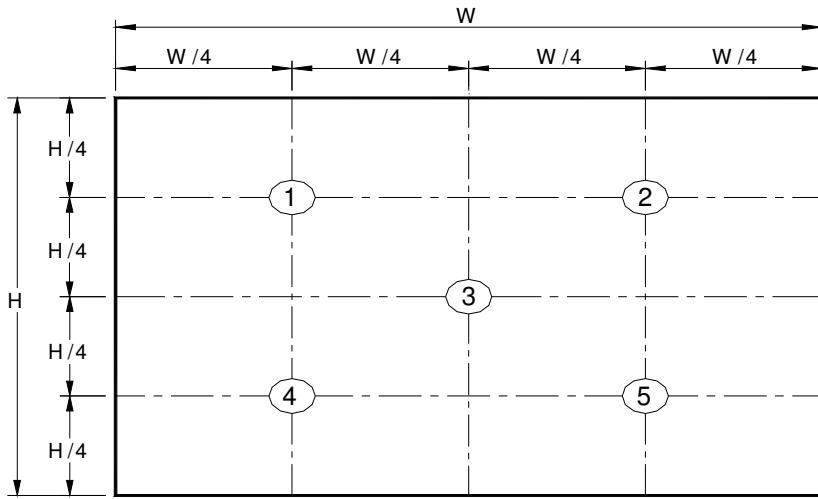
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance $I_{LED}=20mA$		5 points average	200	220	-	cd/m^2	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	32.5	35	-	degree	4, 9
	θ_L		32.5	35	-		
	ϕ_H	Vertical (Upper) CR = 10 (Lower)	27.5	30	-		
	ϕ_L		27.5	30	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	-		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		600	800	-		4, 6
Cross talk	%		-	-	4		4, 7
Response Time	T_r	Rising	-	12	17	msec	4, 8
	T_f	Falling	-	4	8		
	T_{RT}	Rising + Falling	-	16	25		
Color / Chromaticity Coordinates	Red	Rx	0.615	0.645	0.675		4
		Ry	0.305	0.335	0.365		
	Green	Gx	0.285	0.315	0.345		
		Gy	0.580	0.610	0.640		
	Blue	Bx	0.110	0.140	0.170		
		By	0.040	0.060	0.080		
	White	Wx	0.300	0.313	0.326		
		Wy	0.316	0.329	0.342		
NTSC	%		67	72	-		



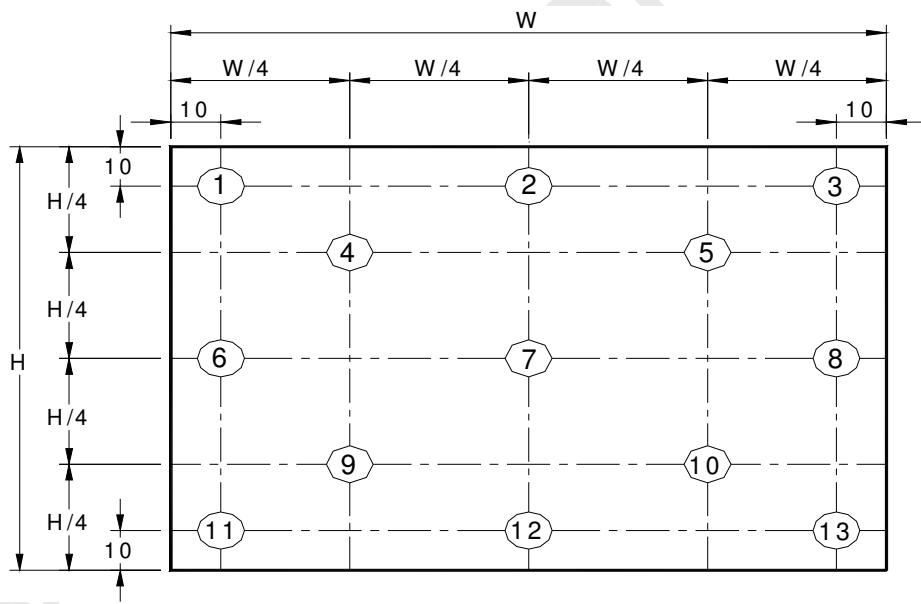
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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

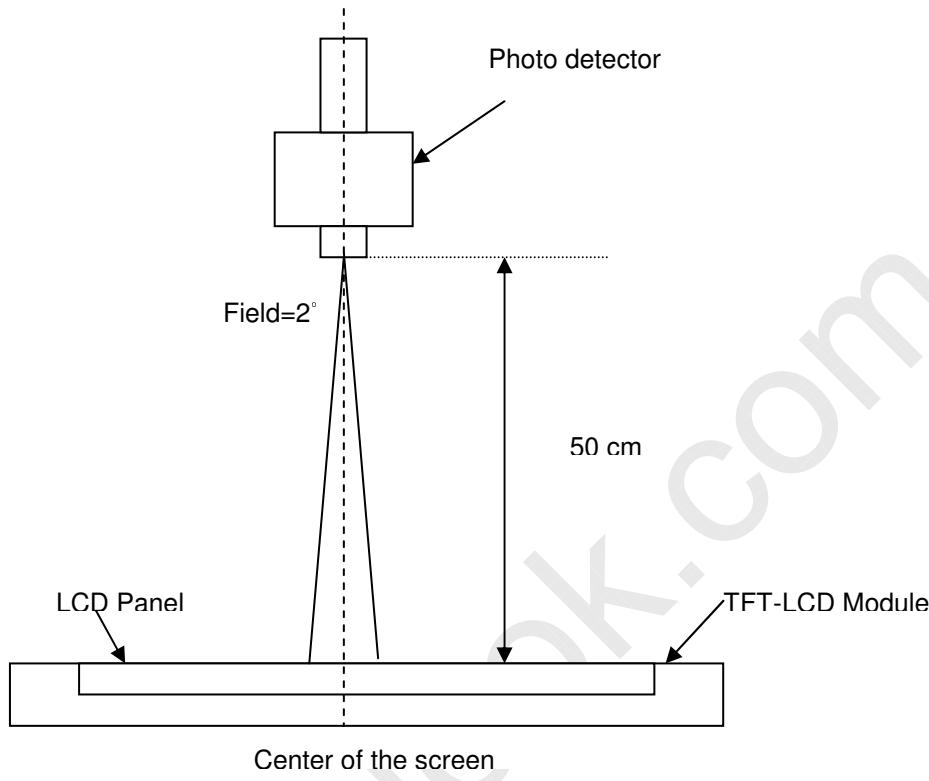
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting



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Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1)+L(2)+L(3)+L(4)+L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

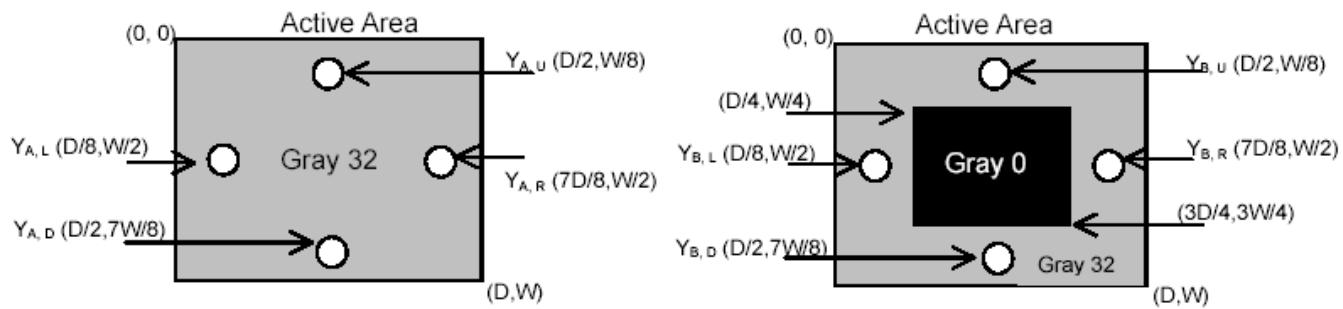
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



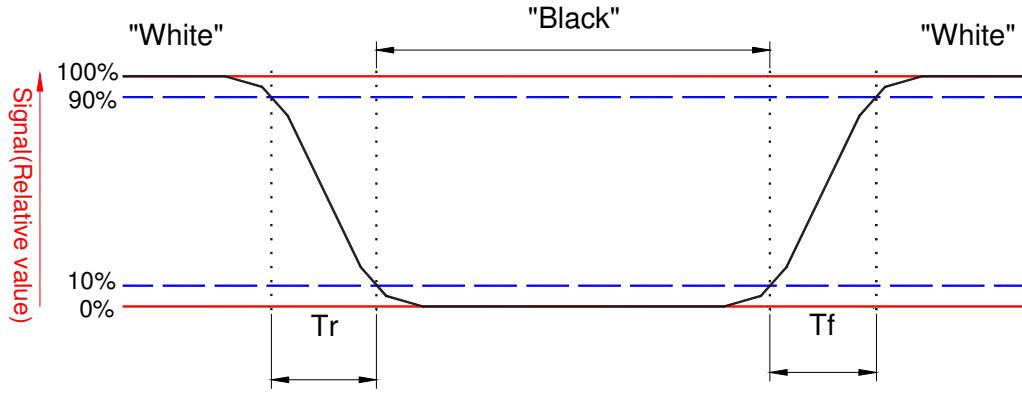
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Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



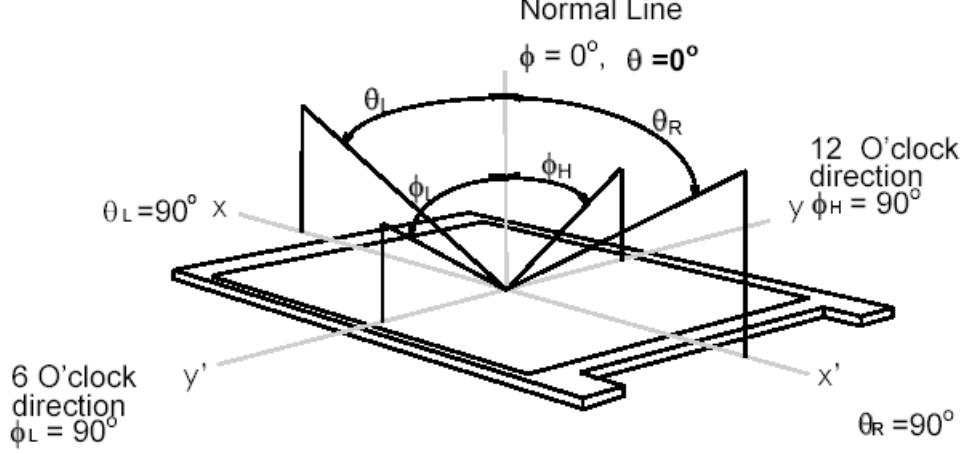


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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



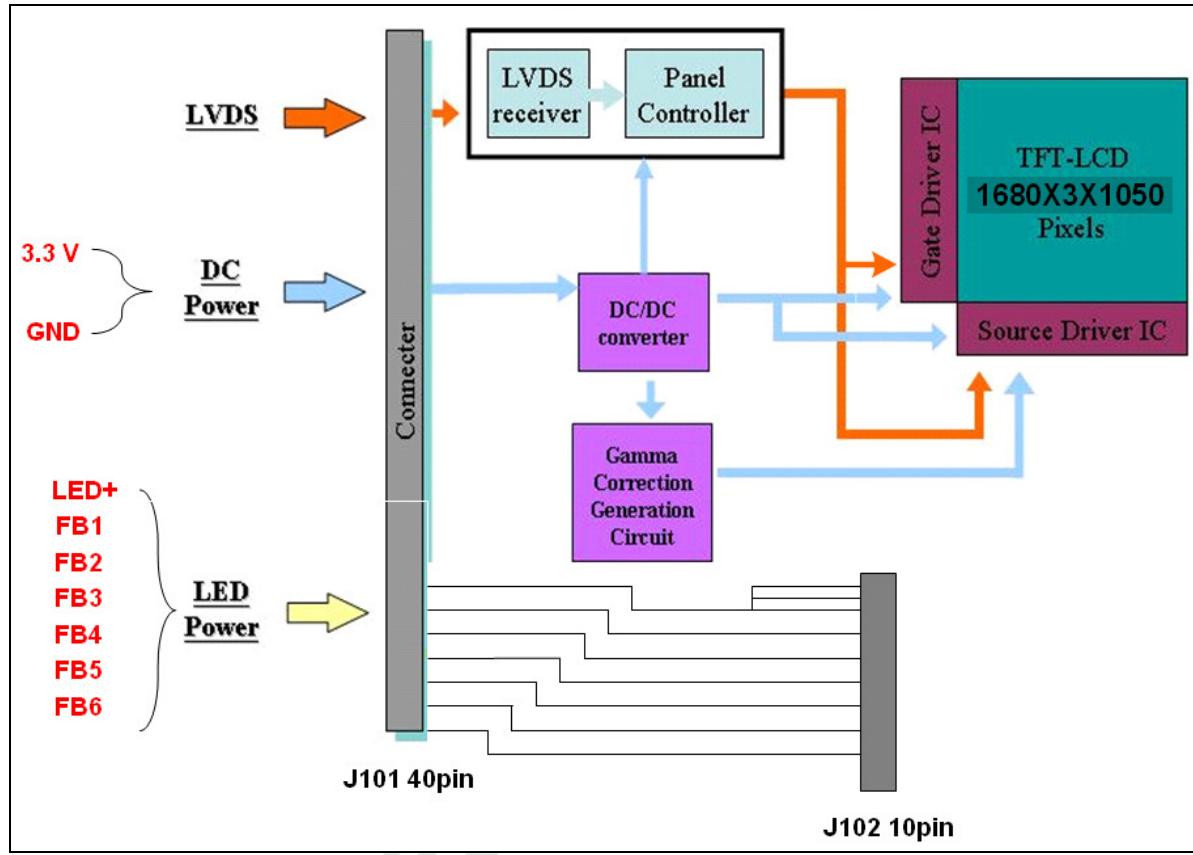


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3. Functional Block Diagram

The following diagram shows the functional block of the 15.4 inches wide Color TFT/LCD 40 Pin one channel Module





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V _{in}	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

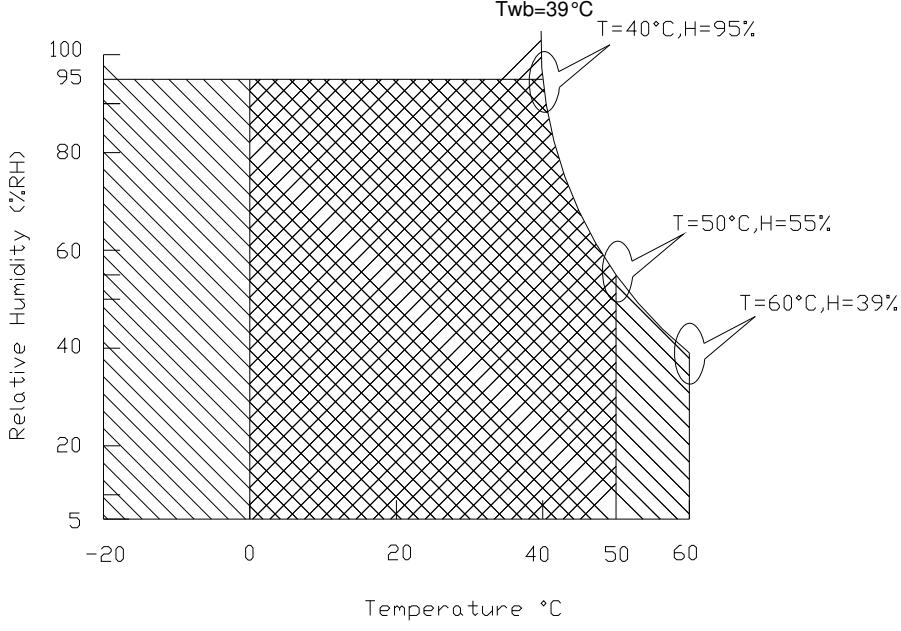
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range

+



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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

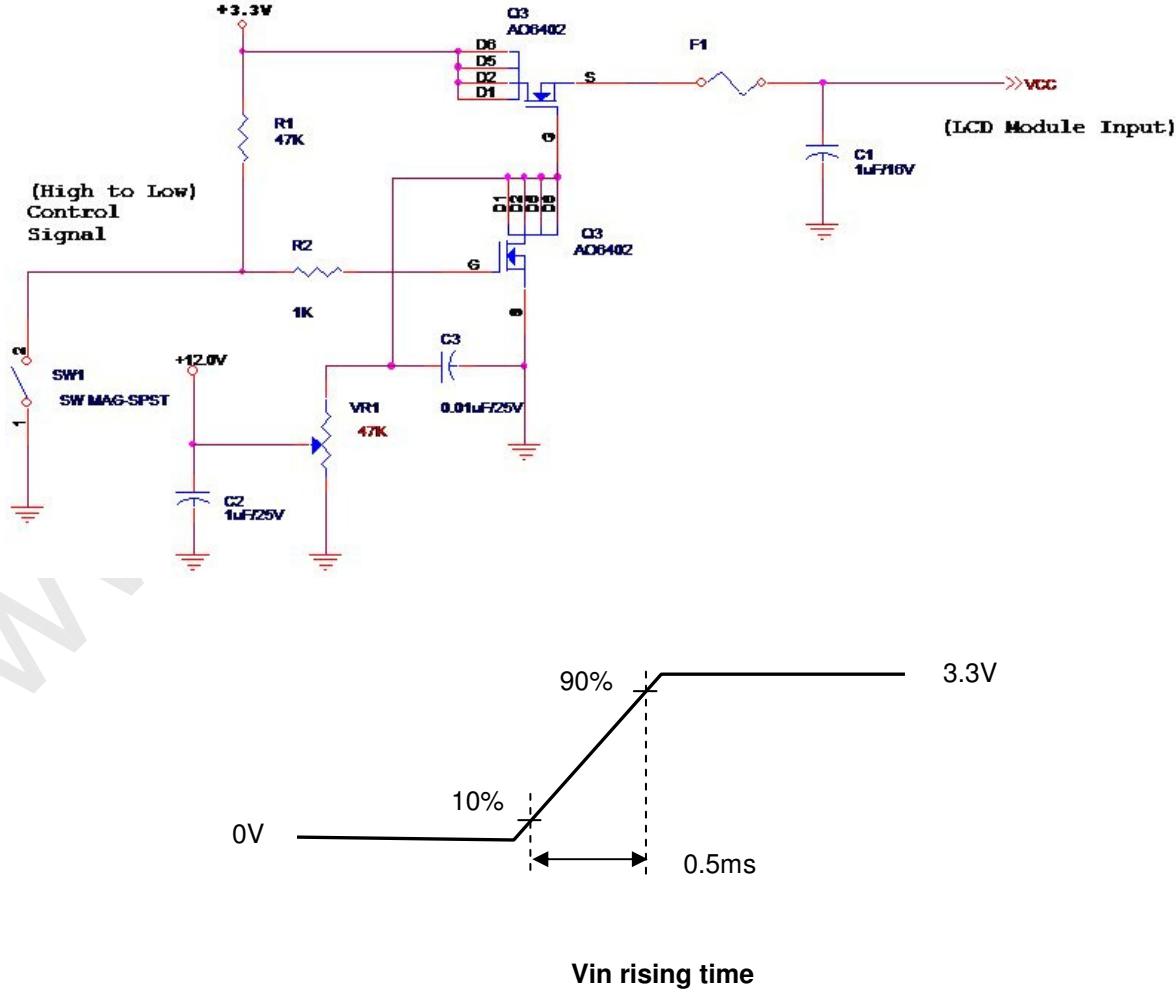
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.2	[Watt]	Note 1
IDD	IDD Current	-	363	400	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDRp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition





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5.1.2 Signal Electrical Characteristics

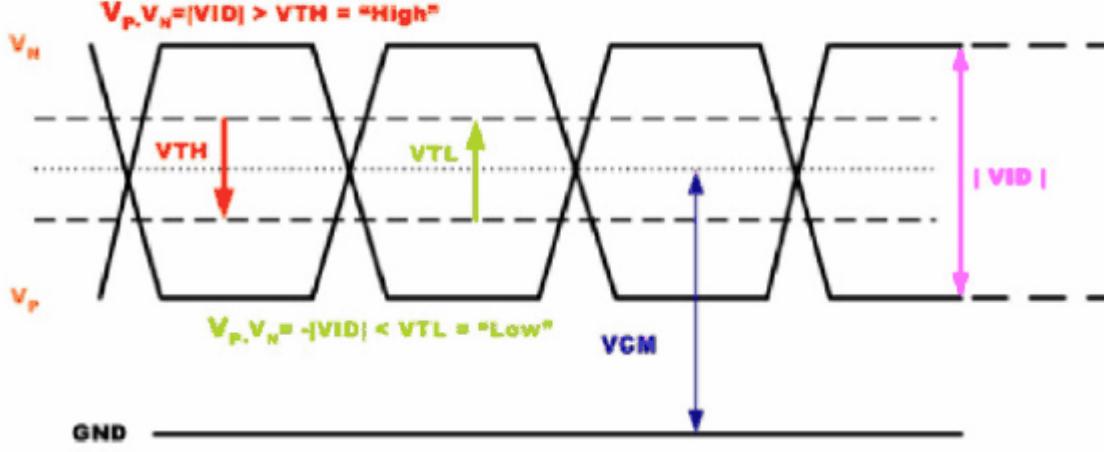
Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold ($V_{cm}=+1.2V$)	-	100	[mV]
V_{tl}	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform

Single-end Signal





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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	4.38	-	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C), Note 2 I _F =20 mA
LED Forward Voltage	VF	2.8	-	3.0	[Volt]	(Ta=25°C) Note 1
LED Forward Current	IF		35		[mA]	(Ta=25°C) Note 1

Note 1: Calculator value for reference $P_{LED} = VF \text{ (Normal Distribution)} * IF \text{ (Normal Distribution)} / \text{Efficiency}$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.



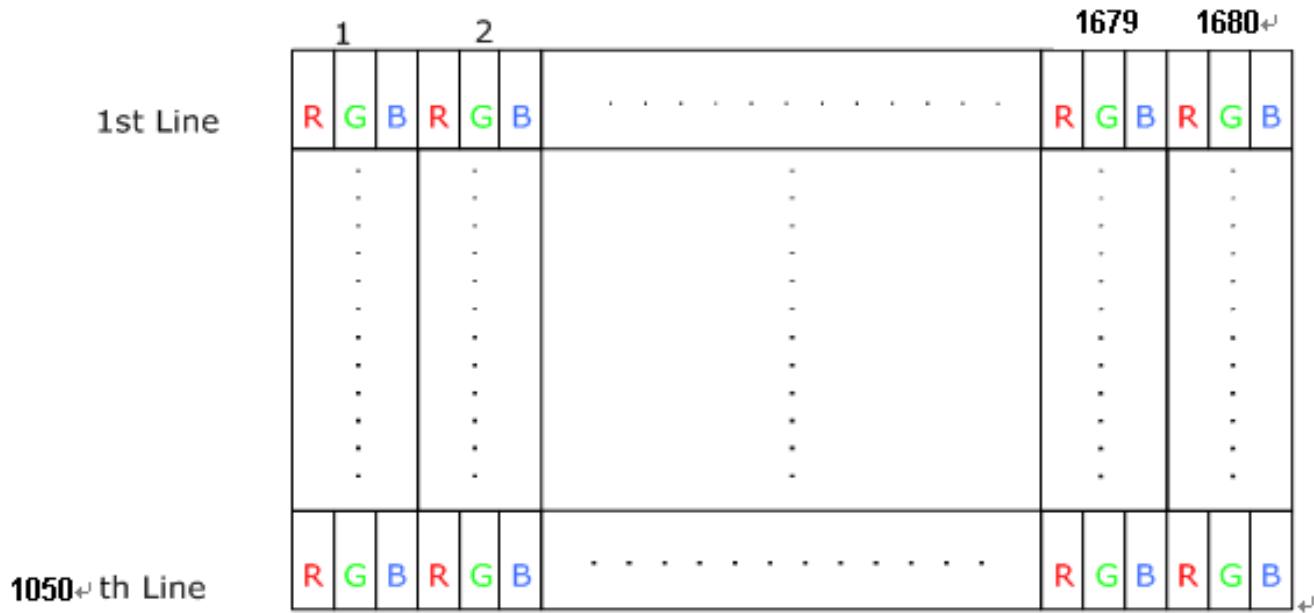
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6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

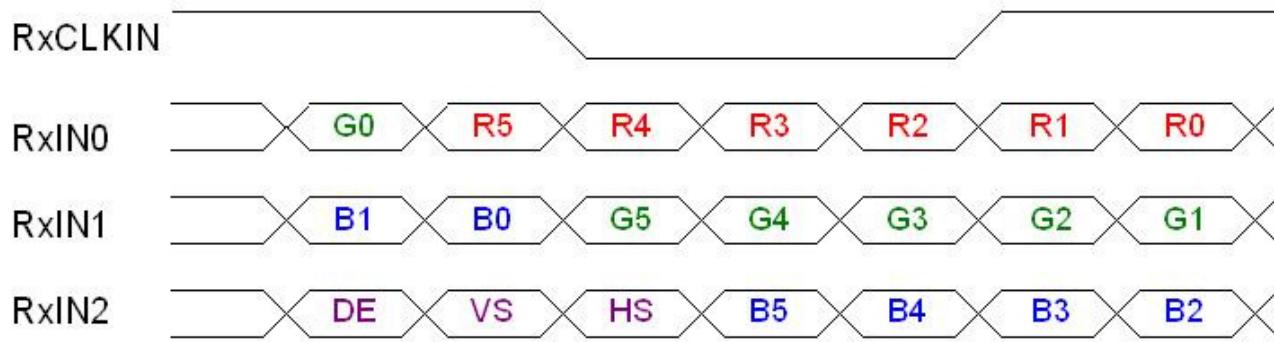




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6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



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6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20474-040E-12 or compatible
Mating Housing/Part Number	IPEX 20472-040T or compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

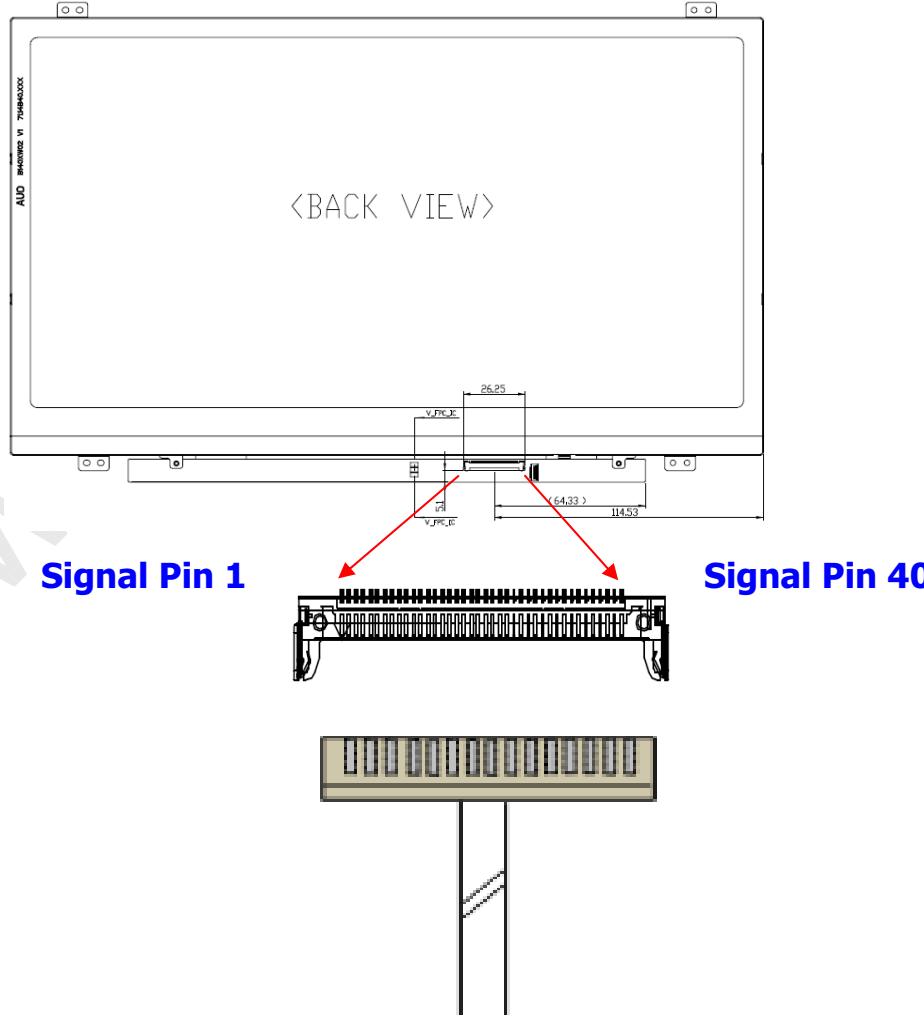
PIN #	SIGNAL NAME	DESCRIPTION
1	GND	GND
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V EEDID	DDC 3.3V power
5	Vsync	Vsync
6	Clk EEDID	DDC Clock
7	DATA EEDID	DDC Data
8	Odd_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
9	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
10	VSS	Ground – Shield
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
13	VSS	Ground – Shield
14	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
16	VSS	Ground – Shield
17	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
18	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
19	VSS	Ground – Shield
20	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (even pixels)
21	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (even pixels)
22	VSS	Ground – Shield
23	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (even pixels)



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24	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (even pixels)
25	VSS	Ground – Shield
26	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
27	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
28	VSS	Ground – Shield
29	Even_ClkIN-	- LVDS differential clock input (even pixels)
30	Even_ClkIN+	+ LVDS differential clock input (even pixels)
31	VDC1	LED Cathode (Negative)
32	VDC2	LED Cathode (Negative)
33	VDC3	LED Cathode (Negative)
34	VDC4	LED Cathode (Negative)
35	VDC5	LED Cathode (Negative)
36	VDC6	LED Cathode (Negative)
37	NC	NC
38	VDDLED	7.5V – 21V LED power
39	VDDLED	7.5V – 21V LED power
40	VDDLED	7.5V – 21V LED power





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Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

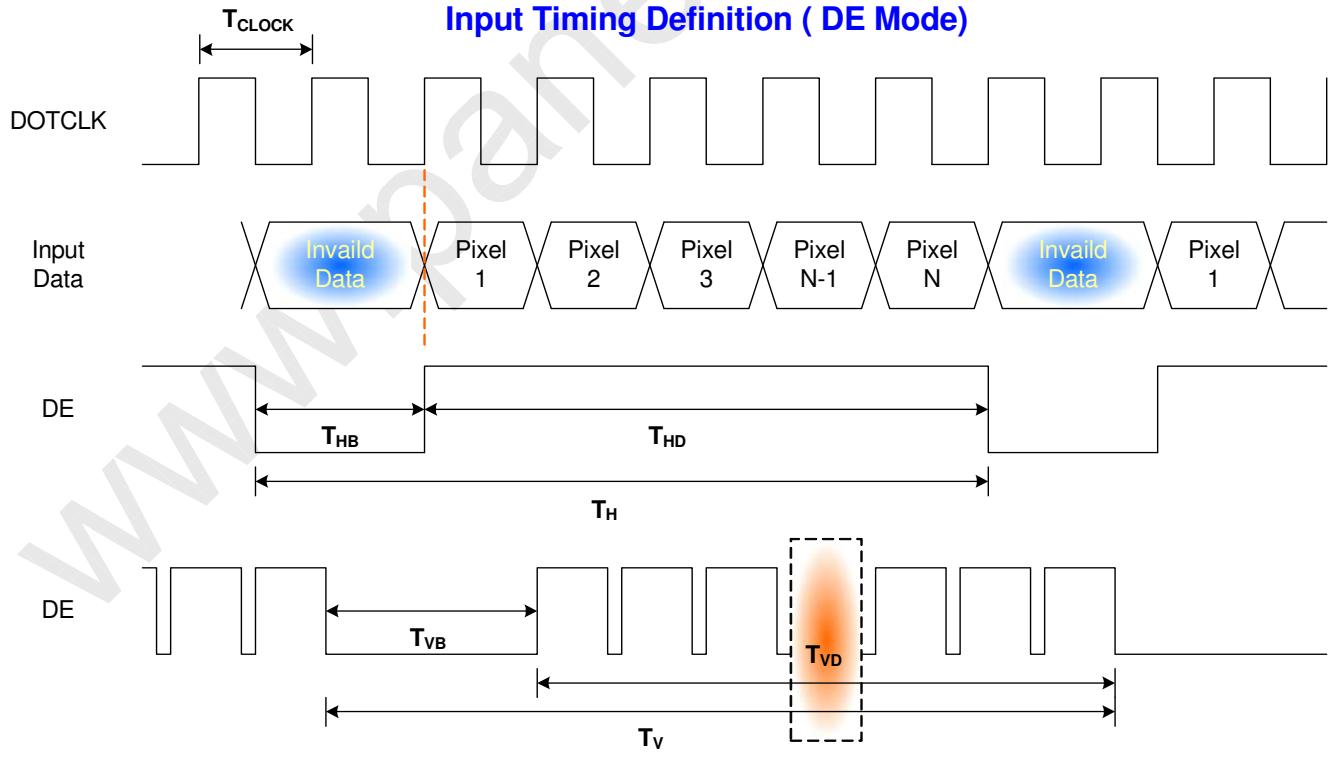
6.4.1 Timing Characteristics

Basically, interface timings should match the 1680x1050/60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frame Rate	-	-	60	-	Hz
Clock frequency	$1/T_{Clock}$	-	119.3	-	MHz
Vertical Section	Period	T_V	-	1080	T_{Line}
	Active	T_{VD}		1050	
	Blanking	T_{VB}	-	30	
Horizontal Section	Period	T_H	-	1840	T_{Clock}
	Active	T_{HD}		1680	
	Blanking	T_{HB}	-	160	

Note : DE mode only

6.4.2 Timing diagram



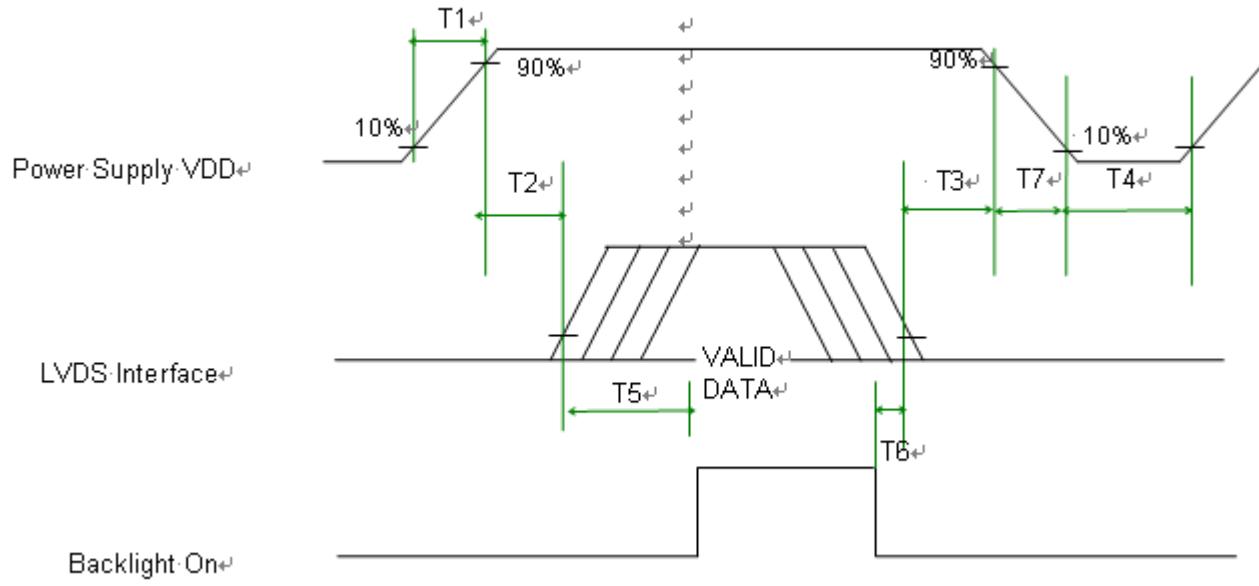


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6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	
T3	0	-	50	
T4	400	-	-	
T5	200	-	-	
T6	200	-	-	
T7	0	-	10	



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7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 3.0 G
- Frequency: 5 - 150Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 65°C, 300h	
Low Temperature Storage	Ta= -25°C, 300h	
Thermal Shock Test	Ta=-25°C to 65°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

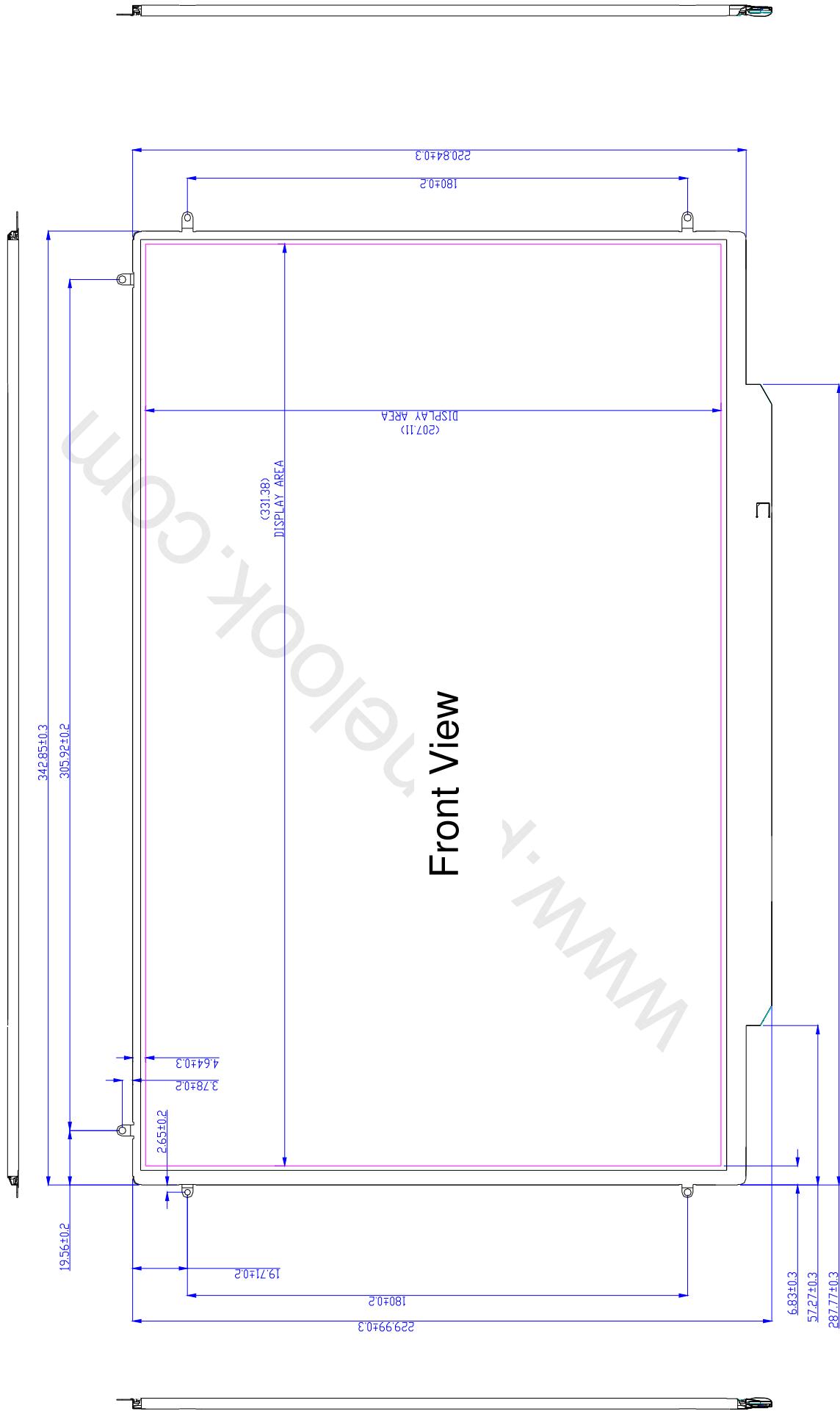
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

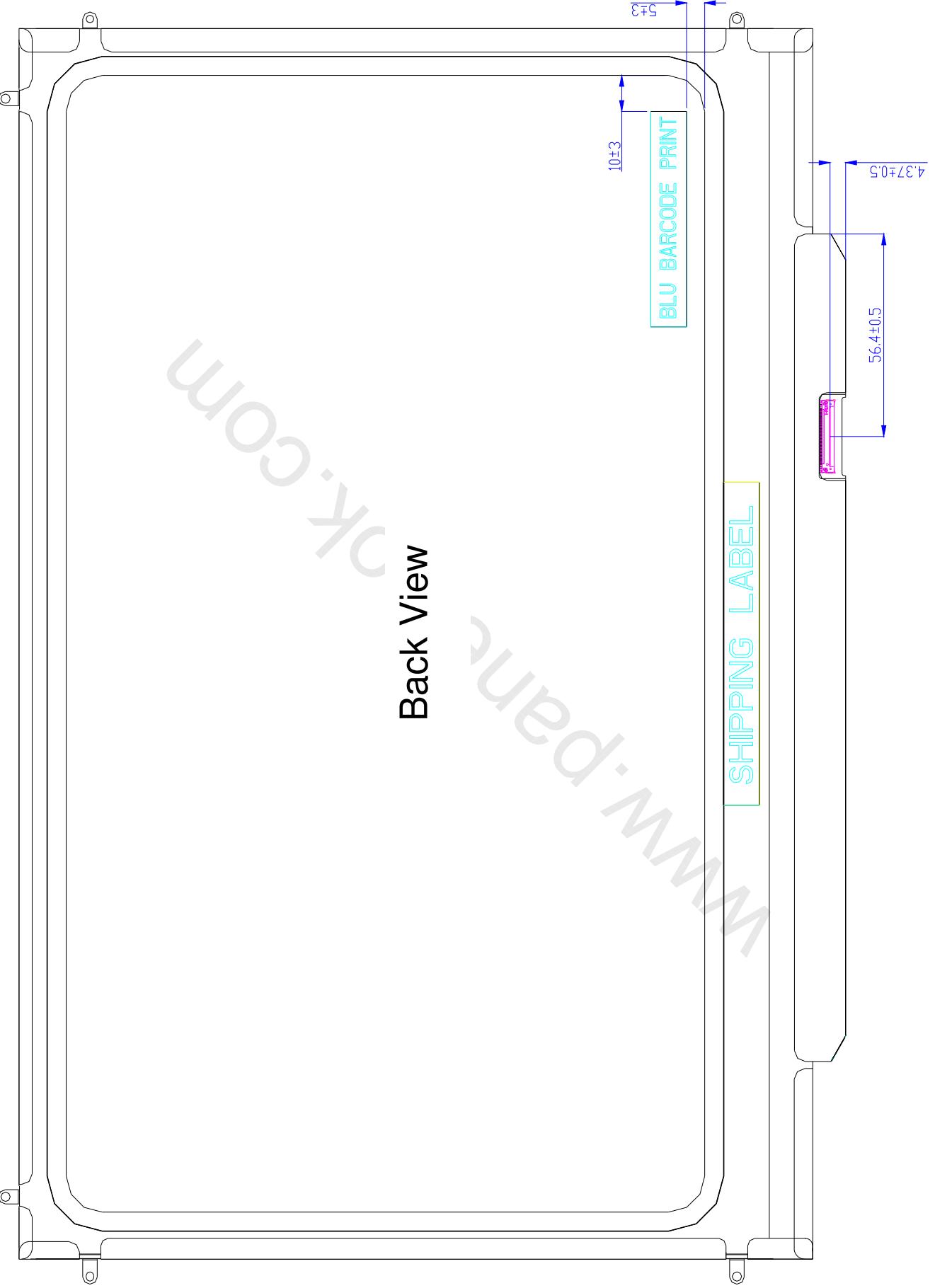
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension





Back View

9. Shipping and Package

9.1 Shipping Label Format

B154SW02 V3

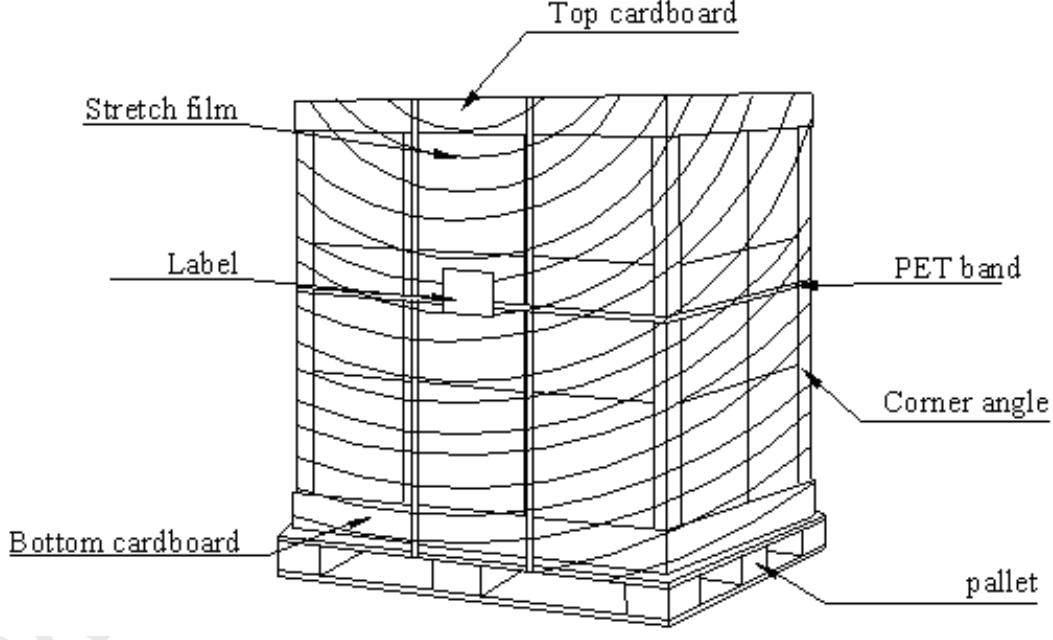
Size: 9mm x 90mm



9.2 Carton Package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm

9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

FUNCTION	B154SW02 V1	Value	Value	Release time	2009/3/30 14:49
	HEX	BIN	DEC		Note
Header					
00	00000000	0	0		
FF	11111111	255	255		
FF	11111111	255	255		
FF	11111111	255	255		
FF	11111111	255	255		
FF	11111111	255	255		
00	00000000	0	0		
EISA Manuf. Code LSB	06	00000110	6	APP9CB9	
Compressed ASCII	10	00010000	16	0 00001(A) 10000(P) 10000(D)	
Product Code	B9	10111000	195	9 CDB (apple assigned code)	
hex LSB first	9C	10011100	156		
32-bit ser #	01	00000001	1	unused	
01	00000001	1	1		
01	00000001	1	1		
01	00000001	1	1		
Week of manufacture	17	00010111	23	Week 31	
Year of manufacture	13	00010011	19	19(2009-1990-19)	
EDID Structure Ver.	01	00000001	1		
EDID revision #	03	00000011	3		
Video input definition	80	10000000	128	Digital Input	
Max H image size	21	00100001	33	33.1cm	
Max V image size	15	00010101	21	20.7cm	
Display Gamma	78	01110000	120	Gamma 2.2	
Feature support	0A	00001010	10	no DPMS, Active off RGB color	
Red/green low bits	F5	11110101	245		
Blue/white low bits	95	10010101	149		
Red x/ high bits	A3	10100011	163		
Red y	55	01010101	85	Rx=0.640	
Green x	4F	01001111	79	Ry=0.340	
Green y	9C	10011100	156	Gx=0.310	
Blue x	26	00100110	38	Gy=0.610	
Blue y	0F	00001111	15	Bx=0.150	
White x	50	01010000	80	By=0.060	
White y	54	01010100	84	Wx=0.313	
Established timing 1	00	00000000	0	Wy=0.329	
Established timing 2	00	00000000	0	unused	
Manufacturer's Timing	00	00000000	0		
Standard timing #1	01	00000001	1		
01	00000001	1	1	unused	
Standard timing #2	01	00000001	1		
Standard timing #3	01	00000001	1		
Standard timing #4	01	00000001	1		
Standard timing #5	01	00000001	1		
Standard timing #6	01	00000001	1		
Standard timing #7	01	00000001	1		
Standard timing #8	01	00000001	1		
Pixel Clock/10,000 (LSB)	9A	10011010	154	Timing Descriptor #1	
Pixel Clock/10,000 (MSB)	2E	00101110	46	1680x1050 @60_mode:pixel clock=119.3MHz	
Horiz. Active pixels(Lower 8 bits)	90	10010000	144	Horiz active=1680 pixels	
Horiz. Active pixels(Horiz. Blanking (Upper4:4 bits))	A0	10100000	160	Horiz blanking=160 pixels	
Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	40	01000000	64		
Vert. Sync. Offset=xx lines, Sync Width=xx lines	30	00110000	48	Vertical active=1050 lines	
Horz. Ver. Sync/Width (upper 2 bits)	20	00100000	32	Vertical blanking=30 lines	
Horz. Image size (Lower 8 bits)	36	00110110	54		
Vert. Image size (Lower 8 bits)	4B	01001011	75	Horiz sync. Offset=48 pixels	
Hor. Image size (Upper 4 bits)	CF	11001111	207	Horiz sync. Pulse Width=32 pixels	
Hor. Image size : Vert. Image size (Upper 4 bits)	1D	00010000	16	Verti sync. Offset=3 lines, Sync Width=6 lines	
Detailed timing/monitor descriptor #2	00	00000000	0		
Version	00	00000000	0	Horiz image size = 331 mm	
Apple edid signature	06	00000110	6	Verti image size = 207mm	
Apple edid signature	10	00010000	16	Horizontal Border = 0	
Link Type (LVDS Link,MSB Justified)	30	00110000	48	Vertical Border = 0	
Pixel and link component format (6-bit panel interface)	00	00000000	0	ASCII Data String:B154SW02 V1	
Panel features (No inverter)	00	00000000	0		
00	00000000	0	For apple		
00	00000000	0	For apple		
00	00000000	0			
00	00000000	0			
00	00000000	0			
00	00000000	0			
0A	00000101	10			
20	00100000	32			
Detailed timing/monitor descriptor #3	00	00000000	0		
00	00000000	0	ASCII Data String:B154SW02 V1		
00	00000000	0			
00	00000000	0			
FE	11111110	254			
00	00000000	0			
42	01000010	66	B		
31	00110001	49	I		
35	00110101	53	S		
34	00110100	52	4		
53	01010011	83	S		
57	01010111	87	W		
30	00110000	48	0		
32	00110010	50	2		
20	00100000	32			
56	01010110	86	V		
31	00110000	49	1		
0A	00001010	10			
20	00100000	32			
Detailed timing/monitor descriptor #4	00	00000000	0	Monitor Name: Color LCD	
00	00000000	0			
00	00000000	0			
FE	11111110	254			
00	00000000	0			
43	01000011	67	C		
6F	01011111	111	o		
6C	01011100	109	l		
6F	01011111	111	o		
72	01100010	114	r		
20	00100000	32			
4C	01001100	76	L		
43	01000011	67	C		
44	01000100	68	D		
0A	00001010	10			
20	00100000	32			
20	00100000	32			
20	00100000	32			
Extension Flag	00	00000000	0		
Checksum	C1	01111110	193		
		SUM	6912		
		SUM to HEX Check	1B00		
			00		